REMARKS

Claims 1-14 are pending. The Examiner's reconsideration of the rejections is respectfully requested in view of the amendments and remarks.

Claim 9 has been objected to for an informality; the Examiner suggested that the term "the set of inverted encryption keys" should read "the set of encryption keys" or "a set of inverted encryption keys."

The term "the set of inverted encryption keys" has been amended to "the set encryption keys in an inverted form." Reconsideration of the objection is respectfully requested.

The Abstract of the Disclosure has been objected to for an informality. The Abstract of the Disclosure has been amended to delete the term "means." Reconsideration of the objection is respectfully requested.

Claims 1-14 have been rejected under 35 USC 103(a) as being unpatentable over USPN 5,473,693 to Sprunk in view of US Patent Publication No. 2002/0048364 to Gilgor et al. The Examiner stated essentially that the combined teachings of Sprunk and Gilgor teach or suggest all of the limitations of Claims 1-14.

Claims 1, 7 and 9 are the independent claims.

Claim 1 claims, *inter alia*, "a second N-round DES device for cryptographically converting the inverted digital input data block into a second digital output data block nonlinearly, based on an input of the set of inverted encryption keys, wherein the first and second

N-round DES devices perform a substantially simultaneous cryptographic conversion process." Claim 7 claims, "cryptographically converting a digital input data block into a first digital output data block nonlinearly, based on an input of a set of encryption keys; inverting the digital input data block and the set of encryption keys; and cryptographically converting the inverted digital input data block into a second digital output data block nonlinearly, based on an input of the inverted encryption keys, wherein the cryptographic conversion processes for obtaining the first and second digital output data blocks are substantially simultaneously performed according to a DES algorithm." Claim 9 claims, *inter alia*, "a second N-round DES device producing a second current pattern during cryptographic process on an inverse of the digital input data block, based on an input of the set encryption keys in an inverted form, wherein the first and second N-round DES devices perform a substantially simultaneous cryptographic conversion processes and wherein the first and second current patterns are inverse patterns, respectively."

Sprunk teaches applying a function to one or more inputs and/or an output of a processor (see FIG 2 and col. 3, line 51 to col. 4, lines 14). Sprunk does not teach or suggest that "the first and second N-round DES devices perform a substantially simultaneous cryptographic conversion" as claimed in Claims 1 and 9, nor "cryptographically converting the inverted digital input data block into a second digital output data block nonlinearly, based on an input of the inverted encryption keys, wherein the cryptographic conversion processes for obtaining the first and second digital output data blocks are substantially simultaneously performed according to a DES algorithm" as claimed in Claim 7. Sprunk teaches only a single processor for performing encryption (see FIG 2). Thus, Sprunk cannot perform a substantially simultaneously cryptographic conversion on a digital input data block and an inverse of the digital input data block. Sprunk does not teach or suggest two encryption devices, much less "the first and second

N-round DES devices perform a substantially simultaneous cryptographic conversion" as claimed in Claims 1 and 9, nor "the cryptographic conversion processes for obtaining the first and second digital output data blocks are substantially simultaneously performed according to a DES algorithm" as claimed in Claim 7. Therefore, Sprunk fails to teach or suggest all the limitations of Claims 1 and 7.

Gilgor teaches parallel block encryption (see Abstract). Gilgor does not teach or suggest that "the first and second N-round DES devices perform a substantially simultaneous cryptographic conversion" as claimed in Claims 1 and 9, nor "cryptographically converting the inverted digital input data block into a second digital output data block nonlinearly, based on an input of the inverted encryption keys, wherein the cryptographic conversion processes for obtaining the first and second digital output data blocks are substantially simultaneously performed according to a DES algorithm" as claimed in Claim 7. For example, Gilgor teaches that different blocks are processed in parallel (see for example, elements 21 in FIGS. 1 and 11). Gilgor does not teach parallel encryption of the digital input data block and an inverse of the digital input data block. Therefore, Gilgor fails to cure the deficiencies of Sprunk.

The combined teachings of Sprunk and Gilgor teach a parallel encryption of different blocks (see Gilgor), wherein inputs and/or an output of the different blocks may be treated by a nonlinear function of Sprunk. The combined teachings of Sprunk and Gilgor fail to teach or suggest that "the first and second N-round DES devices perform a substantially simultaneous cryptographic conversion" on a digital input data block and an inverse of the digital input data block, essentially as claimed in Claims 1, 7 and 9. The Examiner's reconsideration of the rejection is respectfully requested.

Claims 2-6 depend from Claim 1. Claim 8 depends from Claim 7. Claims 10-14 depend

from Claim 9. The dependent claims are believed to be allowable for at least the reasons given for the respective independent claims. Reconsideration of the rejection is respectfully requested.

For the forgoing reasons, the present application, including Claims 1-14, is believed to be in condition for allowance. The Examiner's early and favorable action is respectfully urged.

Respectfully submitted,

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